

Amendments to the Specification

1. Please amend the specification by replacing the paragraph that begins with “A ‘receive component’ ...” at page 5, line 11 (sixth paragraph of the “Summary of the Invention” section)¹ of the specification with the following paragraph:

A “receive component” implements a similar philosophy for the receive direction, *i.e.*, for interfacing a continuous stream of serial TDM data to a network processor for subsequent packetization. The receive component is charged with buffering and assembling received TDM data so as to form bytes of parallel data and present them to the network processor without significant delay. The receive component includes a receive memory comprising a series of memory banks, including at least one “spare” bank for storing incoming data while previously buffered data is transferred in wide-word (parallel) read operations to the network processor. The transmit and receive components are part of an integrated Buffered Interface Component (“BIC”), realized as an FPGA or an ASIC in a present embodiment. The “BIC” also includes logic for directing the buffer memory operations and bus handshaking.

2. At page 8, lines 12-20, replace the paragraph² that begins “Figure 2 is a timing diagram...” with the following paragraph:

Figure 2 is a timing diagram illustrating operation of the H.110 bus, also referred to as the CT (Computer Telephony) bus. H.110 defines the H.100 standard as realized on the compact PCI (cPCI) bus. The main difference between H.100 and H.110 is that H.110 supports compact PCI hot swap. There are four classes of signals on the CT bus: core signals, compatibility signals, optional signals, and reserve signals. The core signals include /CT_FRAME_A frame sync. This is a negative true pulse, nominally 122 nsec wide that straddles the beginning of the first bit of the first time slot. CT_FRAME_A provides the TDM frame sync signal; it has a period of 125 ~~msec~~ microseconds.

¹ Paragraph [0013] in the published version of the application.

² Paragraph [0040] in the published version of the application.

3. At the top of page 9, replace the paragraph³ that begins “Last, in figure 2...” with the following paragraph:

Last, in figure 2, a timing signal (210) illustrates time slots 0-127. As shown, each time slot comprises a single 8-bit data byte (204). Accordingly, each 125 ~~msee~~ microsecond long frame comprises 1024 bits. The first group or time slot following the frame sync is designated CT_Dx; TS0 (data stream x; time slot 0); the second 8 bit group is CT_Dx; TS1 (data stream x; time slot 1) and so on. In a voice application, one channel or phone call travels in an assigned time slot of a selected stream. Thus, the H.110 bus can carry a maximum of 32 times 128 time slots or 4096 simultaneous calls. However, since voice calls require full-duplex operation, each call takes two time slots, so the bus carries 2048 full-duplex calls. Standard digital line speeds – T Carrier and optical – are summarized in Table 1:

4. At page 16, replace the first paragraph with the following paragraph:

In a presently preferred commercial embodiment, the TDM bridge product accommodates a full H.110 bus, i.e. 16 full-duplex streams of voice data, within the timing constraints described. An illustrative memory map for buffering 16 streams is shown in figure 11. This memory would be implemented on board the BIC ASIC chip. In figure 11, a memory (1100) is eight bytes or 64 bits wide, the bytes being numbered 0 to 7 (right to left) at the bottom of the figure. The byte boundaries are illustrated by dashed lines, for example boundaries (1114) and (1116) delineating byte 3. Each 128 rows is delineated by a horizontal line, e.g. (1110), corresponding to one stream of TDM data. Thus, box (1120) shows one TDM frame, i.e. one byte by 128 time slots. Memory 1100 is 1K (1024) rows long, ~~corresponding~~ corresponding to eight streams. A second memory or page 1102 is similarly sized 8 bytes wide by 1K rows or time slots. Thus 16 streams of data can be buffered times 8 bytes or frames. Third and fourth memory pages (1104) and (1106) also are sized 8 bytes wide by 1K rows. This additional memory can be used to buffer another port, such as the SONET port described with reference to figure 14, or can be used as working memory to “double buffer” bus transfers.

³ Paragraph [0041] in the published version of the application.

5. Please replace the paragraph bridging pages 21-22 with the following:

With regard first to figure 7B, packets received from the Ethernet MAC or other packet switched interface (~~730~~) (733) are preliminarily inspected at (705) to detect an administrative (as distinguished from data) packet. Administrative packets are directed to the ARM® (RISC processor) (708) as it handles administrative and configuration tasks for the network processor. One of its tasks is to maintain active call tables (731) in memory. Thus, a packet may be received from a host processor with an instruction to set up (or tear down) a call connection. The ARM updates its map of active channels (731) accordingly. It also uses this information to dynamically provision the TSI as noted earlier; indicated generally in figure 7A as maintaining provisioning data (706). Admin packets can also cause the processor to update system status or alarms (710). These and other communications with the host or system processor (not shown) can be conducted via a common microprocessor bus such as the PCI bus or via a local network. A serial connection (e.g. RS-232) can be provided for communication with the ARM for troubleshooting and for development work in the absence of a host processor.

6. At page 22, at the end of the first paragraph, line 12, insert the following text:

If the received packet is a data packet, the processor determines the type of packet (752), determines the appropriate SDRAM address (754), strips headers (756), and writes the data into the SDRAM (758).